

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

1 1. (Currently Amended) A method of making a multiple gate electrode on a
2 semiconductor device, comprising the steps of:

3 coating a layer of gate electrode material over top and past the opposed sides of
4 a semiconductor device that has been previously coated with a thin film of gate
5 dielectric on the top and the opposed sides of the semiconductor device; and

6 planarizing the layer of gate electrode material to a substantially planar surface of
7 the gate electrode material that extends past each of the opposed sides, prior to
8 patterning the gate electrode material to form a discrete multiple gate electrode on the
9 semiconductor device.

1 2. (Original) The method of claim 1, further comprising the steps of:

2 applying a photoresist mask of substantially uniform thickness on the planar top
3 surface of the planarized gate electrode material;

4 patterning the photoresist mask to cover a corresponding pattern of the discrete
5 multiple gate electrode; and

6 etching the gate electrode material that is uncovered by the photoresist mask to
7 form the discrete multiple gate electrode.

1 3. (Original) The method of Claim 1, further comprising the step of:

2 conforming the layer of gate electrode material with a step height increase
3 corresponding to an increased step height of the semiconductor device.

1 4. (Original) The method of claim 1, wherein the semiconductor device
2 comprises a silicon fin

1 5. (Original) The method of claim 1 wherein, the semiconductor device comprises a
2 fin of silicon and germanium.

1 6. (Original) The method of claim 1, further comprising the steps of:

2 applying a photoresist mask of substantially uniform thickness on the planar top
3 surface of the planarized gate electrode material, the mask comprising photoresist and
4 a mask material selected from the group comprising, silicon nitride, silicon oxynitride,
5 silicon oxide and photo resist, or combinations thereof;

6 patterning the photoresist mask to cover a corresponding pattern of the multiple
7 gate electrode; and

8 etching the gate electrode material that is uncovered by the photoresist mask to
9 form the discrete multiple gate electrode.

1 7. (Original) The method of claim 1, further comprising the steps of:

2 applying a photoresist mask of substantially uniform thickness on the planar top
3 surface of the planarized gate electrode material;

4 patterning the photoresist mask to cover a corresponding pattern of the multiple
5 gate electrode; and

6 plasma etching the gate electrode material that is uncovered by the photoresist
7 mask to form the patterned multiple gate electrode.

- 1 8. (Original) The method as recited in claim 1, further comprising the step of:
2 applying a mask over the planarized surface, wherein the mask is of substantially
3 uniform thickness for accurate patterning thereof.
- 1 9. (Original) The method of claim 1 wherein, the gate dielectric comprises silicon
2 oxide.
- 1 10. (Original) The method of claim 1 wherein, the gate dielectric comprises silicon
2 oxynitride.
- 1 11. (Original) The method of claim 1 wherein, the gate dielectric comprises a high
2 permittivity material.
- 1 12. (Original) The method of claim 1 wherein, the gate dielectric comprises a material
2 having a permittivity greater than 5.
- 1 13. (Original) The method of claim 1 wherein, the gate dielectric comprises a
2 thickness in the range of 3 and 100 Angstroms.
- 1 14. (Original) The method of claim 1 wherein, the multiple gate electrode comprises
2 polycrystalline silicon.
- 1 15. (Original) The method of claim 1 wherein, the multiple gate electrode comprises
2 a conductive material.
- 1 16. (Original) The method of claim 1 wherein, the multiple gate electrode comprises
2 a metal material.
- 1 17. (Currently Amended) A semiconductor device having a multiple gate electrode,
2 comprising:

the semiconductor device having a projecting fin coated with a gate dielectric film over top and opposed sides of the fin;

a multiple gate electrode on ~~more than one side~~ each of the opposed sides of the fin, the multiple gate electrode formed of a layer of gate electrode material and having a substantially planar surface extending over the top and past each of the opposed sides of the fin; and

a patterned mask on the planar surface of the multiple gate electrode, the patterned mask having a substantially uniform thickness and a substantially planar surface.

18. (Currently Amended) The semiconductor device of claim ~~16~~ 17 wherein, the multiple gate electrode is a portion of ~~[[a]]~~ the layer of gate electrode material which has having a planarized surface, ~~and the planarized surface~~ that includes the planar surface of the multiple gate electrode.

19. (Newly Added) A method of making a multiple gate electrode on a semiconductor device, comprising:

providing a semiconductor device over a planar surface that extends from each of opposed sides of the semiconductor device;

coating a top and the opposed sides of the semiconductor device with a thin film gate dielectric;

coating a layer of gate electrode material over the semiconductor device and the planar surface; and

- 9 planarizing the layer of gate electrode material to a substantially planar surface
- 10 formed only of the gate electrode material prior to patterning the gate electrode material
- 11 to form a discrete multiple gate electrode on the semiconductor device.